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[Title of the Invention] ACTIVE MATRIX DISPLAY DEVICE

[Claims]

[Claim 1] A display device using an active matrix light emitting panel including light emitting elements arranged in a matrix, holding circuits each storing and holding a data signal current, driving elements each driving each of the light emitting elements depending on the held voltage, the device characterized by comprising:

setting means for setting a plurality of subfield periods in a unit frame period corresponding to a synchronizing timing of inputted image data;

display controlling means for scanning every row of the light emitting panel in order for each of the subfield periods to make the light emitting elements emit light depending on the inputted image data; and

light emission stopping means for stopping light emission of each of the light emitting elements when a light emitting period of each of the light emitting elements reaches a specified light emitting period in each of a plurality of the subfield periods.

[Claim 2] The display device as claimed in claim 1 characterized in that the light emission stopping means stops the light emission of the light emitting element for each row of the light emitting panel.

[Claim 3] The display device as claimed in claim 1 or 2 characterized in that the light emission stopping means is provided with a timer and a switching circuit that breaks conduction of each of the driving elements depending on an output of the timer.

[Claim 4] The display device as claimed in claim 3 characterized in that the switching circuit is connected in series between the driving element and the holding circuit.

[Claim 5] The display device as claimed in claim 3 characterized in that the switching circuit is connected in parallel to the holding circuit.

[Claim 6] The display device as claimed in claim 3 characterized in that the switching circuit is at least provided with a first switching element connected in series between the driving element and the holding circuit, and a second switching element connected in parallel to the driving element.

[Claim 7] The display device as claimed in claim 3 characterized in that the switching circuit is connected in series to the light emitting element.

[Claim 8] The display device as claimed in any one of claims 1 to 7 characterized in that the specified light emitting period is determined on the basis of a subfield 2^n gradation method.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to an active matrix display device, more particularly to a display device using an active matrix light emitting panel having light emitting elements such as organic electroluminescence elements.

[0002]

[Prior Art]

An organic electroluminescence element (hereinafter referred to as organic EL element) is capable of controlling luminance of light emission thereof by a current flowing in a light emitting element. There are widely carried out developments of matrix displays each using a light emitting panel arranged with such light emitting elements disposed in amatrix. As light emitting panels using such organic EL elements, there are a simple matrix light emitting panel in which organic EL elements are simply disposed in a matrix and an active matrix light emitting panel in which each of organic EL elements disposed in a matrix has an additional driving element including transistors. The active matrix light emitting panel, compared with the simple matrix light emitting panel, has such advantages as to consume less power and cause less crosstalk, which is particularly suited for a large screen display or a high definition display.

[0003] Figure 1 shows an example of a circuit arrangement corresponding to one picture element 10 in a conventional active

matrix light emitting panel. Such a circuit arrangement is disclosed in, for example, Japanese Patent Laid-Open No. 8-241057. In Fig. 1, a gate G of an FET (Field Effect Transistor) 11 (address selection transistor) is connected to an address scanning electrode line (address line) to which an address signal is supplied. Moreover, a source S of the FET 11 is connected to a data electrode line (data line) to which a data signal is supplied. A drain D of the FET 11 is connected to a gate G of an FET 12 (driving transistor) and is grounded through a capacitor 13. A source S of the FET 12 is grounded, a drain D thereof is connected to a cathode of an organic EL element 15 and further connected to a power source through an anode of the organic EL element 15. A controlling operation of the circuit will be explained. First, in Fig. 1, on supplying an "on" voltage to the gate G of the FET 11, the FET 11 flows a current, corresponding to a voltage of data supplied to the source S, from the source S to the drain D. The gate G of the FET 11 at an "off" voltage brings the FET 11 into a so-called "cut off" state to make the drain D of the FET 11 becomes in an "open" state. Therefore, in a period in which the gate G of the FET 11 is at the "on" voltage, the voltage of the source S charges the capacitor 13. The voltage is further supplied to the Gate G of the FET 12, in which a current based on the gate voltage and the source voltage flows from the drain D to the source S through the organic EL element 15 to make the organic EL element 15 emit light.

Moreover, the gate G of the FET 11 becoming at an "off" voltage causes the FET 11 to become in an "open" state, in which the FET 12 keeps the voltage of the gate G by charges stored in the capacitor 13 to maintain a driving current until the next scanning. This also maintains light emission of the organic EL element 15. Incidentally, presence of gate input capacity between the gate G and the source S of the FET 12 allows operation the same as above without providing the capacitor 13.

[0004] The circuit corresponding to one picture element of the display panel is thus arranged in which light emission is controlled by the active matrix driving to maintain the light emission when the organic EL element 15 of the picture element is driven. In each of the picture elements of the above-described active matrix light emitting panel, control of luminance gradation was carried out by an amplitude modulation of the voltage applied to the gate G of the FET 12. Namely, a source-drain current of the FET 12 is varied depending on the voltage applied to the gate G. Thus, by adjusting the magnitude of the voltage applied to the gate G, the amount of the driving current flowing in the organic element 15 can be adjusted. Therefore, instantaneous luminance of the organic EL element was adjusted by adjusting the amount of the driving current of the organic EL element 15.

[0005]

[Problems that the Invention is to Solve]

However, in such a display device that the luminance gradation display is carried out by the amplitude modulation as described above, there was nonlinearity in a relationship between the value of the voltage applied to the gate of the driving FET and the value of the current flowing between the source and the drain, that is, the current to voltage characteristic of the driving FET. This causes variation in the luminance gradation due to variation between characteristics of driving FETs in the display panel plane, which presented problem of causing difficulty in displaying multigradation with high definition.

[0006] The present invention was made in view of this respect with an object of providing an active matrix display device which can present a high definition multigradation display without any variation in luminance gradation over the whole plane of the display panel.

[0007]

[Means for Solving the Problem]

A display device according to the invention is a display device using an active matrix light emitting panel including light emitting elements arranged in a matrix, holding circuits each storing and holding a data signal current, driving elements each driving each of the light emitting elements depending on the held voltage, which is characterized by comprising: setting means for setting a plurality of subfield periods in a unit

frame period corresponding to a synchronizing timing of inputted image data; display controlling means for scanning every row of the light emitting panel in order for each of the subfield periods to make the light emitting elements emit light depending on the inputted image data; and light emission stopping means for stopping light emission of each of the light emitting elements when a light emitting period of each of the light emitting elements reaches a specified light emitting period in each of a plurality of the subfield periods.

[0008] Another characteristic of the invention is in that the light emission stopping means stops the light emission of the light emitting element for each row of the light emitting panel. Moreover, further another characteristic of the invention is in that the light emission stopping means is provided with a timer and a switching circuit that breaks conduction of each of the driving elements depending on an output of the timer. Furthermore, still another characteristic of the invention is in that the switching circuit is connected in series between the driving element and the holding circuit.

[0009] Further characteristic of the invention is in that the switching circuit is connected in parallel to the holding circuit. In addition, still further characteristic of the invention is in that the switching circuit is connected in series to the light emitting element.

[0010]

[Mode for Carrying Out the Invention]

An example of the invention will be explained in detail with reference to the drawings. In the drawings explained in the following, substantially equivalent parts will be designated with the same reference numerals and signs. Figure 2 schematically shows an arrangement of an organic EL display device 20 using an active matrix light emitting panel as a first example of the invention.

[0011] In Fig. 2, an analog/digital (A/D) converter 21 receives an analog image signal input, which is converted to digital image signal data. The digital image signal obtained by the conversion is supplied from the A/D converter 21 to a frame memory 24, in which the digital image signal data are temporarily stored frame by frame. Meanwhile, a display controlling unit (hereinafter referred to as controller) 26, carrying out control of various parts in the organic EL display device 20, controls the digital image signal data stored in the above frame memory 24 by using a column address counter 2 and a row address counter 23. The control of the digital image signal data are carried out by providing a plurality of subfields (in the following, explanation will be made by taking an example about the case of providing eight subfields) each with a different light emitting period taken as a parameter. This converts the digital image signal data to a plurality of (here, eight) gradation display data each being supplied to a multiplexer 25 together

with light emitting data or non-light-emitting data corresponding to an address of a picture element in a light emitting panel 30.

[0012] Moreover, the controller 26 carries out control so that, of the light emitting data or non-light- emitting data supplied to the multiplexer 25, column data corresponding to each of the sub fields are made held in a data latch circuit provided in a column driver 28 sequentially from the first row in the order of the arrangement of the picture elements. The controller 26 then supplies the column data for each subfield, held by the data latch circuit in order, to the light emitting panel 30 row by row. Along with this, the controller 26 makes a row driver 27 carry out simultaneous light emission of a series of picture elements in a row corresponding to the row with the supplied column data. Furthermore, the controller 26 has a time measuring device (timer) inside (not shown) for controlling a light emission controlling driver 31 to control a light emitting period of each of the picture elements for each of the subfields. The operation is carried out for each of subfields from a first subfield to an eighth subfield (here, carried out eight times) for each of which data of one frame are supplied with column data taken row by row. Each of the picture elements in the light emitting panel 30 is subjected to light emission control by a specified period as will be explained later for each of the provided subfields to allow a light emitting display to be

performed with multigradation display.

[0013] Incidentally, as shown in Fig. 3, in the example, one frame period for the inputted image signal is divided into eight subfields, in each of which relative ratios of luminance is set so as to be 1/2,1/4, 1/8, 1/16, 1/32, 1/64, 1/256 (that is, from the first subfield to the eighth subfield in order). By selectively combining such subfields, a luminance gradation display (that is, a display by a method based on the subfield 2^n gradation method) with 256 ways is possible.

[0014] The organic EL display device according to the invention is thus arranged, in which, for analog image signals being inputted, light emission control is repeated for each subfield by carrying out scanning all of the addresses in the light emitting panel. This allows light emitting display with multigradation display to be carried out frame by frame. Figure 4 shows a circuit arrangement corresponding to one picture element of an active matrix light emitting panel as the first example of the invention. The example differs from the circuit arrangement of the conventional art shown in Fig. 1 in that a switching circuit 32 is provided between a connection point of the source S of the FET 11 for selecting address with the capacitor 13, and the gate G for the driving FET 12. The switching circuit 32 is provided for controlling light emission and non-light-emission (stopping light emission) of the organic EL element 15 by controlling conduction of the driving FET 12.

The switching circuit 32 is provided with two FETs 33 and 34 carrying out switching in response to a light emission controlling signal from the light emission controlling driver 31 described later. In the switching circuit 32, the FET 33 is connected between the connection point of the source S of the FET 11 with the capacitor 13 and the gate G of the FET 12. The FET 34 is connected between the gate G of the FET 12 and the ground (GND). Therefore, when the FET 33 is made conducting and the FET 34 is made nonconducting, the switching circuit 32 carries out light emission control for making the organic EL element 15 emit light (ON). In the reverse case, the light emission control is carried out to make the light emission of the organic EL element 15 stop (OFF).

[0015] In the following, an operation of light emission control will be explained with reference to time charts shown in Fig. 5 and Fig. 6. In the light emission control, the controller 26 controls light emission or non-light-emission of the light emitting panel 30 on the basis of the digital image signal data stored in the frame memory 24. First, the controller 26, on supply of the digital image signal data to the frame memory 24, writes the digital image signal data of one frame in the frame memory 24. Next, the controller 26 outputs an instruction for outputting data for the first subfield (SF1) to the multiplexer 25. The controller 26 then outputs an instruction for specifying the first row to the row address counter 23 and, along with

this, outputs an instruction for specifying the first column to the column address counter 22.

[0016] This makes digital image data of one frame at the specified address (the first row and the first column) converted to eight gradation display data each corresponding to each of the subfields, which are supplied to the multiplexer 25 in order as data including light emission data or non-light-emission data corresponding to addresses of the picture elements in the light emitting panel 30. Of the data for the specified address (the first row and the first column) supplied to the multiplexer 25, the controller 26 makes the data in the first subfield outputted to the column driver 28. In the column driver 28, the data are held by a data latch circuit (not shown) provided in the column driver 28.

[0017] Following this, the controller 26 outputs an instruction to the column address counter 22 for updating the column by one. Namely, the instruction of specifying the second column is outputted to the column address counter 22. This makes an address (the first row and the second column) designated to repeat the same operation as that when the previously explained address (the first row and the first column) was specified. In this way, the controller 26 makes the above explained operation repeated to each column in the first row in order to thereby make the data of all columns in the first row held in the data latch circuit provided in the column driver 28.

[0018] After all of the column data in the first row were latched, as shown in Fig. 5, the controller 26 makes each of the column data in the first row written in a picture element in each column corresponding to the data. Namely, the FET 11 for selecting address corresponding to each picture element is made conducting. At the same time, the controller 26 controls the light emission controlling driver 31 to supply a control signal for making the switching circuit 32 conducting (light emission control ON), and to make an organic EL element of a picture element, having data indicating light emission, emit light. In addition, the controller 26, when a specified light emitting period (T_{L1}), predetermined for the first subfield, has passed, supplies a signal indicating to stop light emission of the above organic EL element to the light emission controlling driver 31. The light emission controlling driver 31 supplies control signals for stopping light emission of the organic EL elements (light emission OFF) to all of the switching circuits 32 in the first row to bring the organic EL elements in non-light-emitting state.

[0019] The controller 26, as the step after all of the column data in the first row are latched, outputs an instruction for specifying the second row to the row address counter 23 and, along with this, outputs an instruction for specifying the first column to the column address counter 22. In the same way as that in the case of the above described operation for

the first row, control is carried out so that data latch is carried out about all of the column data in the second row. After all of the column data in the second row have been latched, in the same way as that in the case of the above described operation for the first row, a light emission controlling operation is carried out about a picture element in each column in the second row.

[0020] The controller 26, by carrying out such operations over all of the rows (namely, the first line to the m-th line), can carry out light emission control of all of the picture elements in the light emitting panel 30 with the light emission of the picture elements made in correspondence with the data in the first subfield. Then, the controller 26 produces an instruction to the multiplexer 25 to output data of the second subfield. From this and later, the controller 26 repeats the same operations as that in the case of the above explained first subfield to carry out light emission corresponding to the data for the second subfield.

[0021] In this way, there is carried out light emission corresponding to the first subfield to the eighth subfield. Moreover, the invention is characterized by having means for stopping light emission of the light emitting elements after a specified light emitting period has passed for each subfield. Therefore, it is possible to allot any given light emitting period shorter than the address period (T_A) to the subfield.

Namely, without means for stopping light emission, it is impossible to allot a light emitting period shorter than the address period to the subfield. This is because light emission of a light emitting picture element can not be stopped until the light emission of the picture element is updated by starting of the address period for the next subfield. Thus, the next subfield cannot be started until the completion of the address period, the period necessary for scanning all of the rows.

[0022] Figure 5 shows the case in which light emission in each line is controlled with a light emitting period shorter than an address period (T_A) in the k-th subfield ($1 \leq k \leq 8$). By the controller 26 carrying out the same control as those explained before, light emission in each row is controlled with a specified light emitting period (T_{LK}) determined for the subfield. For example, when one frame is displayed with 60 Hz, one frame lasts for about 16.7 milliseconds (ms). Here, an explanation will be made about an example in which an address period is taken as 0.84 ms (40 % of one frame period × 1/8), and a light emitting period in the first subfield (1/2) is taken as a value equal to or less than 1/2 the one frame period, for example, 5ms. At this time, light emitting periods of subfields subsequent to the second sub field become 2.5 ms, 1.25 ms, 0.625 ms, ..., 0.039 ms as $1/2^1$, $1/2^2$, $1/2^3$, ..., $1/2^7$, respectively. Therefore, in this case, the light emitting periods in the subfields subsequent to the fourth subfields (the fourth subfield to the

eighth subfield) are shorter than the address period (T_A = 0.84 ms). Nevertheless, a control is carried out to each subfield so that it has a desired light emitting period.

[0023] At the time when the display control from the first subfield to the eighth subfield is finished in such ways as described above, display of one frame is completed. The controller 26 thereafter updates the data stored in the frame memory 24 to the data corresponding to the next frame to carry out next display control. Therefore, according to the invention, the above-explained control for stopping light emission makes it possible to control light emission for each subfield with any given light emitting period shorter than the address period, which allows a display with wide gradation.

[0024] Figure 7 shows a circuit arrangement corresponding to one picture element of an active matrix light emitting panel as the second example of the invention. The example differs from the first example in that a switching circuit 32 is provided with an FET 35 connected in parallel to the capacitor 13. Namely, a drain D of the FET 35 is connected to a connection point of the source S of the FET 11 with the capacitor 13, and a source S is grounded. Therefore, when the FET 35 is made conducting in response to a control signal supplied to the gate G, light emission of the organic EL element 15 is stopped.

[0025] Figure 8 shows a circuit arrangement corresponding to one picture element of a light emitting panel as the third

example of the invention. The example differs from the above-explained example in that a switching circuit 32 is provided with an FET 36 connected in series between the capacitor 13 and the gate G of the FET 12. Namely, a drain D of the FET 36 is connected to a connection point of the source S of the FET 11 with the capacitor 13, and a source S is connected to the gate G of the FET 12. Therefore, when the FET 36 is made nonconducting in response to a control signal supplied to the gate G, light emission of the organic EL element 15 is stopped.

[0026] Each of Figs. 9 to 11 shows a circuit arrangement corresponding to one picture element of a light emitting panel as each of other examples of the invention. Each of the examples differs from the above-explained examples in that a switching circuit 32 is provided with an FET 37 connected in series to the organic EL element 15. Namely, when the FET 37 is made nonconducting in response to a control signal supplied to the gate G, light emission of the organic EL element 15 is stopped.

[0027] As described above, according to the invention, the above-explained control for stopping light emission makes it possible to control light emission for each subfield with any given light emitting period shorter than the address period, which allows realization of a display with wide gradation. Numerical values shown in the above-described examples are only examples which can be adequately changed. Furthermore, various kinds of the switching circuits can be used in being adequately

combined.

[0028]

[Advantage of the Invention]

As is apparent from the above description, according to the invention, light emitting period in each subfield can be arbitrarily controlled. This makes it possible to realize an active matrix display device which can present a high definition multigradation display without any variation in luminance gradation over the whole plane of the display panel.

[Brief Description of the Drawings]

[Fig. 1] A view showing an example of a circuit arrangement corresponding to one picture element in a conventional active matrix light emitting panel;

[Fig. 2] A view schematically showing an arrangement of an organic EL display device using an active matrix light emitting panel as a first example of the invention;

[Fig. 3] A view showing one frame period, subfield periods, and address periods of a digital image signal;

[Fig. 4] A view showing a circuit arrangement corresponding to one picture element of an active matrix light emitting panel as the first example of the invention;

[Fig. 5] A time chart showing timing of light emission control carried out for each subfield by a controller;

[Fig. 6] A time chart showing control timing with which the controller carries out control of light emission with a

light emitting period shorter than the address period;

[Fig. 7] A view showing a circuit arrangement corresponding to one picture element of an active matrix light emitting panel as the second example of the invention;

[Fig. 8] A view showing a circuit arrangement corresponding to one picture element of a light emitting panel as the third example of the invention;

[Fig. 9] A view showing a circuit arrangement corresponding to one picture element of a light emitting panel as another example of the invention;

[Fig. 10] A view showing a circuit arrangement corresponding to one picture element of a light emitting panel as another example of the invention; and

[Fig. 11] A view showing a circuit arrangement corresponding to one picture element of a light emitting panel as another example of the invention.

[Description of the Reference Numerals and Signs in the Principle Parts]

10 picture element

11 address selecting FET

12 driving FET

13 capacitor

15 light emitting element

20 display device

21 A/D converter

22 column address counter

23 row address counter

24 frame memory

25 multiplexer

26 controller

27 row driver

28 column driver

30 light emitting panel

31 light emission controlling driver

32 switching circuit

33, 34, 35, 36 FET

[Abstract]

[Object] To provide an active matrix display device which can present a high definition multigradation display without any variation in luminance gradation over the whole plane of the display panel.

[Means for Resolution] The device comprises setting means for setting a plurality of subfield periods in a unit frame period corresponding to a synchronizing timing of inputted image data, display controlling means for scanning every row of the light emitting panel in order for each of the subfield periods to make the light emitting elements emit light depending on the inputted image data, and light emission stopping means for stopping light emission of each of the light emitting elements when a light emitting period of each of the light emitting elements reaches a specified light emitting period in each of the subfield periods, in the case in which address period, as a period that light emission controlling means requires for scanning all of the rows of the light emitting panel, is longer than a specified light emitting period.

Fig. 1

10 one picture element

15 EL element

Aj address line

Bj data line

common electrode

Fig. 2

image signal

22 column address counter

23 row address counter

24 frame memory

25 multiplexer

26 controller

27 row driver

28 column data driver

30 light emitting panel

31 light emission controlling driver

Fig. 3

address period

subfield (SF1)

frame period

Fig. 4

15 organic EL element

Aj address line

Bj data line

control signal

control signal

common electrode

Fig. 5

scanning signal

first line

light emission control

subfield period (SF1)

light emitting period = T_{L1}

second line

light emission control

m-th line

light emission control

address period = T_A

Fig. 6

scanning signal

first line

light emission control

subfield period (SF_{-K})

light emitting period = T_{LK}

second line

light emission control

m-th line

light emission control

address period = T_A

Fig. 7

Aj address line

Bj data line

control signal

common electrode

Fig. 8

15 organic EL element

Aj address line

Bj data line

control signal

common electrode

Fig. 9

15 EL element

Aj address line

Bj data line

control signal

common electrode

Fig. 10

15 EL element

Aj address line

Bj data line

control signal

common electrode

Fig. 11

one picture element

15 EL element

Aj address line

Bj data line

control signal

common electrode